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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, DUSTIN	
ART UNIT	PAPER NUMBER
2154	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/923,976	BRESNIKER ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/15/2006 has been entered.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 3-11, 13, 14, 16-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As per claims 1, 11 and 14, it only appears to be producing a tangible result which enables any usefulness of having determined the shutdown process when the processor has provided the graceful shutdown signal. Under all other conditions, the final result achieved is a determination which has not been used nor made available for use in the disclosed practical application [i.e. there is no tangible result if the

processor has not provided the graceful shutdown signal]. As such, no usefulness of having made the determined can be realized. Therefore, the claims do not provide a tangible result.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 6, 9-15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berg et al. [US Patent No 6,598,175] in view of Bilir [US Patent No 5,923,099].

6. As per claim 1, Berg discloses the invention as claimed including a host processor card configured to be fitted into a server system [i.e. circuit packs that are mounted in a circuit pack carrier] [111, 112, Figure 1; and col 3, lines 3-14], the host processor card comprising:

a processor [101, Figure 1; and col 3, lines 10-14];

a memory coupled to the processor for storing an operating system [102, Figure 1; and col 3, lines 11-14];

a power control line for controlling the power state of the host processor card [i.e. electrical signal] [col 3, lines 44-50; and col 4, lines 60-64]; and

a graceful shutdown circuit coupled to the processor and the power control line [i.e. control circuit generates a message requesting operating system to shutdown and restart] [133, Figure 1; and col 3, lines 46-58], the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal [col 4, lines 11-27].

Berg does not specifically disclose

the processor configured to automatically provide a graceful shutdown signal to the graceful shutdown circuit based on a status of the operating system.

Bilir discloses

the processor configured to automatically provide a graceful shutdown signal to the graceful shutdown circuit based on a status of the operating system [i.e. determination is made whether the operating system has issued a shutdown complete signal indicating that the shutdown task have been successfully performed] [41, Figure 2; and col 3, lines 35-48].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Berg and Bilir because Bilir's teaching of determining operating system status would guarantee that the automatically shut down operations in a graceful, nondisruptive manner and implement system shutdown only after ascertaining that it is safe to do so [Bilir, col 1, lines 35-42].

7. As per claim 2, Berg does not specifically disclose wherein the graceful shutdown circuit is configured to allow an immediate shutdown of the host processor card when a received power

control signal indicates that the host processor card is to be powered down if the processor has not provided the graceful shutdown signal. Bilir discloses wherein the graceful shutdown circuit is configured to allow an immediate shutdown of the host processor card when a received power control signal indicates that the host processor card is to be powered down if the processor has not provided the graceful shutdown signal [i.e. terminating provision of backup power at the expiration of either the first or second timer] [14, Figure 2; col 2, lines 6-8; and col 6, lines 3-5]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Berg and Bilir because the teaching of Bilir would guarantee that the automatically shut down operations in a graceful, nondisruptive manner and implement system shutdown only after ascertaining that it is safe to do so [Bilir, col 1, lines 35-42].

8. As per claim 6, Berg does not specifically disclose wherein the processor includes a register for indicating when a graceful shutdown is to be performed, and wherein the operating system is configured to write a value to the register indicating whether a graceful shutdown is to be performed. Bilir discloses wherein the processor includes a register for indicating when a graceful shutdown is to be performed, and wherein the operating system is configured to write a value to the register indicating whether a graceful shutdown is to be performed [i.e. communication registers] [34, Figure 3; and col 4, lines 35-col 5, lines 15]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Berg and Bilir because Bilir's teaching of registers would allow to store and maintain status information for proper operations to prevent system corruption.

9. As per claim 8, Berg discloses wherein the graceful shutdown circuit further comprises a monitor circuit coupled to the power control line and coupled to the processor, the monitor circuit configured to provide an indication of the status of the power control line to the processor [i.e. watchdog] [134, Figure 1; and col 3, lines 58-col 4, lines 8].

10. As per claim 9, Berg does not specifically disclose a switch circuit coupled to the power control line and coupled to the processor, the switch circuit configured to override a power down signal on the power control line and thereby maintain power to the host processor card if the processor has provided the graceful signal to the graceful shutdown circuit. Bilir discloses a switch circuit coupled to the power control line and coupled to the processor, the switch circuit configured to override a power down signal on the power control line and thereby maintain power to the host processor card if the processor has provided the graceful signal to the graceful shutdown circuit [i.e. the main AC power restoration, and abort the shutdown process] [col 3, lines 49-59]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Berg and Bilir because Bilir's teaching of restoration of power would allow the system to revert to the initial state and obviate the need for any shutdown [Bilir, col 3, lines 49-58].

11. As per claim 10, Berg discloses a manual emergency switch coupled to the switch circuit, the emergency switch configured to cause immediate shutdown of the host processor card [i.e. pushbutton switch] [Abstract; and col 3, lines 15-23].

12. As per claim 11, it is rejected for similar reasons as stated above in claims 1, 8 and 9.

13. As per claim 12, it is rejected for similar reasons as stated above in claim 2.

14. As per claim 13, it is rejected for similar reasons as stated above in claim 10.

15. As per claim 14, it is rejected for similar reasons as stated above in claims 1, 8 and 9.

16. As per claim 15, it is rejected for similar reasons as stated above in claim 2.

17. As per claim 19, it is rejected for similar reasons as stated above in claim 6.

18. As per claim 20, it is rejected for similar reasons as stated above in claim 10.

19. Claims 3-5, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berg et al. [US Patent No 6,598,175] in view of Bilir [US Patent No 5,923,099], and further in view of Hamre et al. [US Patent No 5,530,302].

20. As per claim 3, Berg and Bilir do not specifically disclose wherein the power control line is coupled to a switch that is configured to close when the host processor card is inserted into the server system, causing the power control line to indicate that the host processor card is to be

power up. Hamre discloses wherein the power control line is coupled to a switch that is configured to close when the host processor card is inserted into the server system, causing the power control line to indicate that the host processor card is to be power up [Abstract; and col 3, lines 5-19]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Berg, Bilir and Hamre because Hamre's teaching would provide hot-swapping modules for digital systems which can be inserted and removed without interrupting data bus communications [Hamre, col 2, lines 46-49].

21. As per claim 4, Berg discloses wherein the switch is configured to open when the host processor card is being removed from the server system, causing the power control line to indicate that the host processor card is to be powered down [col 4, lines 33-42].

22. As per claim 5, Berg discloses wherein the power control line is coupled to a server management card that is configured to control the power state of the host processor card via the power control line when the switch is closed [i.e. maintenance processor] [103, Figure 1; and col 3, lines 28-30].

23. As per claims 16-18, they are rejected for similar reasons as stated above in claims 3-5.

24. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berg et al. [US Patent No 6,598,175] in view of Bilir [US Patent No 5,923,099], and further in view of Crawford et al. [US Patent Application No 2002/0138772].

25. As per claim 7, Berg and Bilir do not specifically disclose wherein the operating system is configured to write a value to the register indicating that a graceful shutdown is to be performed when the operating system boots up to a point that an immediate shutdown should not be performed. Crawford discloses wherein the operating system is configured to write a value to the register indicating that a graceful shutdown is to be performed when the operating system boots up to a point that an immediate shutdown should not be performed [i.e. during boot-up, the power manager configures registers] [paragraphs 0056-0063]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Berg, Bilir and Crawford because Crawford's teaching would allow to store and maintain status information for proper operations to prevent system corruption.

26. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

27. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dustin Nguyen
Examiner
Art Unit 2154